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10/805,106	03/19/2004	Mariano G. Fernandez	008410.P19207	8494
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/805,106	FERNANDEZ ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Phillip H. Nguyen	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 16 January 2009.

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-36 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-36 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____ .	6) <input type="checkbox"/> Other: _____ .

## **DETAILED ACTION**

1. This action is in response to the amendment filed 1/16/2009.
2. Claims 1-36 remain pending in this application.

### ***Response to Arguments***

3. Applicant's arguments filed 1/16/2009 have been fully considered but they are not deemed persuasive.

### **Applicants argue that Stotzer fails to teach:**

1. determining one instruction in the program preceding a determined NOP instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed; and replacing the determined NOP instruction with the determined instruction preceding the determined NOP instruction.
2. deleting an NOP instruction in the program that is not needed to provide a processing delay to ensure the data available to at least one dependent instruction without moving a non-NOP instruction.
3. after deleting the at least one instruction, replacing at least one NOP instruction with one determined instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed.

4. determining whether the accessed NOP instruction is needed to delay processing of one dependent instruction following the accessed NOP instruction to ensure that data is available to the dependent instruction accessing the data.
5. a determination of an instruction to move forward whose movement forward will not result in data not being available to one dependent instruction following the NOP instruction.
6. moving one instruction forward to replace an NOP instruction and making the claimed determination when deciding whether to move the instruction forward.

Examiner respectfully disagrees with all the allegations as argued.

1. Stotzer's approach is directed to reduce the size of code by deleting NOP instructions inserted to compensate for instruction latencies. In one embodiment, Stotzer teaches "**a method according to an embodiment of this invention may include the steps of locating (i.e. determining) delayed effect instructions followed by NOPs, such as load or branch instructions, within a code (i.e. load or branch instructions are instructions in the program preceding determined NOP instructions whose movement forward to replace the determined NOP instruction will not result in data not being available when needed), deleting the NOPs from the code, and inserting a NOP field into the delayed effect instructions**" (see at least Para [0067]). The NOP instructions within the code are dummy instructions that have no effect. They may be used as an explicit "do nothing" instructions that are necessary to compensate for latencies in the instruction pipeline. However, such NOP instructions increase code

size. Therefore, Stotzer reduces the code size by deleting the NOP instruction within the code and insert the NOP field into the delayed effect instructions. The NOP field defines the following latency following the load or branch instructions. By inserting NOP field into the delayed effect instructions, the NOP instructions are no longer needed to provide the processing delay and therefore have been deleted to reduce the code size. The replacement of the NOP instructions with delayed effect instructions will not result in data not being available when needed because NOP instructions were inserted to compensate for instruction latencies.

2. As discussed above, by inserting NOP field into the delayed effect instructions, the NOP instructions are no longer needed to provide the processing delay and therefore have been deleted to reduce the code size.

3. As discussed above, Stotzer reduces the code size by replacing the NOP instructions with delayed effect instructions such as load or branch instructions with NOP field inserted. The replacement of the NOP instructions with delayed effect instructions will not result in data not being available when needed because NOP instructions were inserted to compensate for instruction latencies.

4. As discussed above, NOP instructions were inserted into the code by the programmer to compensate for instruction latencies. However, such NOP instructions increase the code size. Stotzer's approach is to minimize the code size by deleting the unneeded NOP instructions and replacing it with delayed effect instructions with NOP field inserted.

5. As discussed above, the delayed effect instruction such as load or branch instruction are located and the replacement of the NOP instruction with delayed effect instructions will not result in data not being available when needed because NOP instructions were inserted to compensate for instruction latencies.

6. Stotzer further teaches “***A method for reducing total code size according to this invention may comprise the steps of determining a latency (i.e. number of NOP instructions) between a defining instruction, such as a load instruction (LD), and a using instruction, such as an arithmetic instruction (i.g., ADD), to perform a pipelined operation...A NOP field then may be inserted into the at least one of the defining and using instructions***” (see at least Para [0040]). In other words, a determination is made whether to move forward the delayed effect instruction to replace the NOP instruction based on the number of determined latency between the delayed effect instruction and the arithmetic instruction.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Stotzer et al. (EP1113356A2).

As per claims 1, 13 and 24:

Stotzer teaches

accessing a program comprising a plurality of instructions including at least one no operation (NOP) instruction (see at least *FIG. 1 - instructions are fetched from cache or memory into a processor for executing*);

determining one instruction in the program preceding a determined NOP instruction whose movement forward to replace the determined NOP instruction will not result in data not available when needed (see at least [0067] "*locating delayed effect instructions followed by NOPs, such as load or branch instructions, within a code*"; see also [0045-0063] – *all the examples 1b, 2b, 1c, etc.*); and

replacing the determined NOP instruction with the determined instruction preceding the determined NOP instruction (see at least [0067] "*deleting the NOPs from the code*").

As per claims 2, 14 and 25:

Stotzer further teaches

deleting one NOP instruction in the program that is not needed to provide a processing delay to ensure that data is available to at least one dependent instruction without moving a non-NOP instruction (see at least [0067] "*deleting the NOPs from the code*" - *the NOPs are no longer needed and therefore have been deleted from the code*).

As per claims 3, 15 and 26:

Stotzer further teaches

deleting at least one NOP instruction in the program that is not needed to provide the processing delay to ensure the data is available to at least one dependent instruction (see at least [0067] “*deleting the NOPs from the code*”).

after deleting the at least one instruction, replacing at least one NOP instruction with one determined instruction preceding the at least one NOP instruction, whose movement forward to replace the determined NOP instruction will not result in data not being available when needed (see at least [0045-0063] – *see the examples 1b, 2b, 1c, etc.*).

As per claims 4, 16 and 27:

Stotzer further teaches

performing an additional iteration of deleting at least one instruction and then replacing the at least one NOP instruction in response to replacing at least one NOP instruction (see at least [0045-0063] – *see the examples 1b, 2b, 1c, etc.*).

As per claims 5, 17 and 28:

Stotzer further teaches

wherein the instructions in the program comprise assembly language instructions coded by a developer (see at least [0008] “*Pipelining is a method for executing instructions in an assembly-line fashion*”).

As per claims 6, 18 and 29:

Stotzer further teaches

determining whether the accessed NOP instruction is needed to delay processing of one dependent instruction following the accessed NOP instruction to ensure that data is available to the dependent instruction accessing the data (see at least [0067] “*locating delayed effect instructions followed by NOPs, such as load or branch instructions, within a code*”); and

deleting the accessed NOP instruction in response to determining that the NOP instruction is not needed to ensure that data is available to the dependent instruction accessing the data (see at least [0067] “*deleting the NOPs from the code*” – *the NOPs are no longer needed and therefore have been deleted from the code*).

As per claims 7, 19 and 30:

Stotzer further teaches

identifying instructions preceding the NOP instruction that have a delay in writing the results and identifying dependent instructions following the NOP instruction that are dependent on an availability of data from the identified

instructions having the delay in writing the results (see at least [0003] “*Delayed effect instructions are instructions, in which one or more successive instructions may be executed before the initial instructions effects are complete. NOP instructions are inserted to compensate for instruction latencies*”).

As per claims 8, 20 and 31:

Stotzer further teaches

wherein the determining of one instruction in the program to move forward comprises determining one instruction whose movement forward to replace the determined NOP instruction will not result in data not being available to one dependent instruction following the NOP instruction (see at least [0067] “*locating delayed effect instructions followed by NOPs, such as load or branch instructions, within a code; deleting the NOPs from the code*”; see also [0045-0063] – *all the examples 1b, 2b, 1c, etc.*”)

As per claims 9, 21 and 32:

Stotzer further teaches

wherein the one previous instruction comprises a preceding instruction closest to the accessed NOP instruction in the program (see also [0045-0063] – *all the examples 1b, 2b, 1c, etc.*”).

As per claims 10, 22 and 33:

Stotzer further teaches

deleting at least one NOP instruction not needed to ensure that data accessed by the dependent instruction is available to the dependent instruction, wherein the operations of replacing accessed NOP instructions with previous non-NOP instructions are performed after deleting NOP instructions not needed to ensure that data accessed by the dependent instruction is available (see at least [0045-0063] – *all the examples 1b, 2b, 1c, etc.*).

As per claims 11, 23 and 34:

Stotzer further teaches

wherein the determined instruction is further not a branch target instruction (see at least [0045] “*LD instruction*”).

As per claims 12, 24 and 35:

Stotzer further teaches

wherein the program instructions are for execution by an engine in a multiprocessor engine (see at least *FIG. 1*).

As per claim 36:

Stotzer further teaches

determining whether the instruction to move forward causes the data needed by one dependent instruction to be written in fewer cycles such that the number of cycles between a writing instruction and the dependent instruction are not sufficient to guarantee that the written data will be available to the dependent instruction (see at least [0045-0063] – *all the examples 1b, 2b, 1c, etc.*)

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip H. Nguyen whose telephone number is (571) 270-1070. The examiner can normally be reached on Monday - Thursday 10:00 AM - 3:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

3/29/2009

/Wei Y Zhen/

Supervisory Patent Examiner, Art Unit 2191